REMARKS

Reconsideration and allowance of the above referenced application are respectively requested.

Claims 21-23, 37 and 43 stand rejected under 35 USC 112, first paragraph as allegedly not being supported by the specification. These claims have been cancelled in order to obviate this rejection.

Multiple enumerated claims, including claim 1, were rejected under 35 USC 103(a) as allegedly being unpatentable over Ha in view of Ota. Claim 1 has been amended to obviate the rejection. Amended claim 1 recites that the pair of regions is formed of the same material as the channel region, and that each of the pair of regions have a first portion that is contiguous to the channel region and a second portion that is contiguous to the source or drain regions. The regions 32E and 32A in Ha may correspond to these first and second portions. However, the LDD region 32A of Ha is not formed of the same material as the channel region, because this region 32A is doped with an impurity as shown in Figure 4D. The channel region is not doped with such an impurity; for example see column 4 lines 31-50 and the LDD regions 32A of Figure 4G in U.S. Patent 5,767,530.

In addition to the above, new claims 45 and 46 recite that a distance between the first portion and the source or drain region, that is a width of the second portion, is larger than the thickness of the first conductive layer. New claims 47 and 48 recite that a distance between the first portion and a source or drain regions (that is a width of the second region) is equal to or less than the thickness of the first conductive layer. These features are supported by the present specification for example page 8 line 11 through page 11 line 5. Moreover, Ha in view of Ota do not disclose or suggest these features. For these reasons, it is respectfully suggested that these rejections are overcome.

In view of the above amendments and remarks, all of the claims should be in condition for allowance. A formal notice to that effect is respectfully solicited.

Enclosed is a $516.00 check for excess claim fees and a $410.00 check for the Petition for Extension of Time fee. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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Attached is a marked-up version of the changes being made by the current amendment.

Version with markings to show changes made

In the claims:

Please cancel claims 6-8, 11-13, 15-18, 20-23, 33-37 and 39-43 as follows.

Pease amend claim 1 as follows.

1. [Amended] A semiconductor device comprising:

a semiconductor [layer] region comprising a source region, a drain region, [and] a channel region [formed on an insulating surface], and a pair of regions between the channel region and the source and drain regions, said pair of regions formed of a same material as said channel region wherein each of said pair of regions has a first portion contiguous to the channel region and a second portion contiguous to the source or drain regions;

a gate insulating film formed [on] over said semiconductor [layer] region;

a first conductive layer formed [on said gate insulating film wherein said first conductive layer extends over said channel region] over the channel region with the gate insulating film interposed therebetween; and

[a first anodic oxide layer formed on at least side surface of said first conductive layer;]

a second conductive layer formed on said first conductive layer[; and] wherein a width of the first conductive layer is narrower than that of the second conductive layer;

wherein the second conductive layer extends beyond side edges of the first conductive layer and extending portions of the second conductive layer overlap the first portions of said pair of regions while the second portions are not overlapped by said second conductive layer

[a second anodic oxide layer formed on at least side surface of said second conductive layer,

wherein each of said first and second conductive layers comprises a material selected from the group consisting of molybdenum, tantalum, aluminum, chromium, nickel, zirconium, titanium, palladium, silver, copper, and cobalt,

wherein an anodization rate of said first conductive layer is greater than that of said second layer so that a width of said first conductive layer is narrower than that of said second conductive layer, and

wherein width between a side edge of said second conductive layer and a side edge of said second anodic oxide layer is 500. to 1000.].

Please add new claims 44-84 as follows.

44. (NEW) A semiconductor device comprising:

a semiconductor film comprising a source region, a drain region, a channel region formed on an insulating surface, and a pair of regions between the channel region and the source and drain regions, said pair of regions formed of a same material as said channel region wherein each of said pair of regions has a first portion contiguous to the channel region and a second portion contiguous to the source or drain regions;

a gate insulating film formed over the semiconductor region;

a first conductive layer formed over the channel region with the gate insulating film interposed therebetween; and

a second conductive layer formed on the first conductive layer wherein a width of the first conductive layer is narrower than a width of the second conductive layer,

wherein the second conductive layer extends beyond side edges of the first conductive layer and extending portions of the second conductive layer overlap the first portions of said pair of regions while the second portions are not overlapped by said second conductive layer.

45. (NEW) A semiconductor device comprising:

a semiconductor region comprising a source region, a drain region, a channel region, and a pair of regions between the channel region and the source and drain regions, said pair of regions are formed of a same material as said channel region, wherein each of said pair of regions has a first portion contiguous to the channel region and a second portion contiguous to the source or drain regions;

a gate insulating film formed over the semiconductor region;

a first conductive layer formed over the channel region with the gate insulating film interposed therebetween; and

a second conductive layer formed on the first conductive layer, wherein a width of the first conductive layer is narrower than a width of the second conductive layer,

wherein the second conductive layer extends beyond side edges of the first conductive layer and extending portions of the second conductive layer overlap the first portions of said pair of regions while the second portions are not overlapped by said second conductive layer, and

wherein a distance between the first portion and the source or drain region is larger than a thickness of the first conductive layer.

46. (NEW) A semiconductor device comprising:

a semiconductor film comprising a source region, a drain region, a channel region formed on an insulating surface, and a pair of regions between the channel region and the source and drain regions, said pair of regions formed of a same material as said channel region wherein each of said pair of regions has a first portion contiguous to the channel region and a second portion contiguous to the source or drain regions;

a gate insulating film formed over the semiconductor region;

a first conductive layer formed over the channel region with the gate insulating film interposed therebetween; and

a second conductive layer formed on the first conductive layer, wherein a width of the first conductive layer is narrower than that of the second conductive layer,

wherein the second conductive layer extends beyond side edges of the first conductive layer and extending portions of the second conductive layer overlap the first portions of said pair of regions while the second portions are not overlapped by said second conductive layer, and

wherein a distance between the first portion and the source or drain region is larger than a thickness of the first conductive layer.

47. (NEW) A semiconductor device comprising:

a semiconductor region comprising a source region, a drain region, a channel region, and a pair of regions between the channel region and the source and drain regions, said pair of regions formed of a same material as said channel region wherein each of said pair of regions has a first portion contiguous to the channel region and a second portion contiguous to the source or drain regions;

a gate insulating film formed over the semiconductor region;

a first conductive layer formed over the channel region with the gate insulating film interposed therebetween; and

a second conductive layer formed on the first conductive layer wherein a width of the first conductive layer is narrower than that of the second conductive layer,

wherein the second conductive layer extends beyond side edges of the first conductive layer and extending portions of the second conductive layer overlap the first portions of said

pair of regions while the second portions are not overlapped by said second conductive layer, and

wherein a distance between the first portion and the source or drain region is equal to or less than a thickness of the first conductive layer.

48. (NEW) A semiconductor device comprising:

a semiconductor film comprising a source region, a drain region, a channel region formed on an insulating surface, and a pair of regions between the channel region and the source and drain regions, said pair of regions formed of a same material as said channel region, wherein each of said pair of regions has a first portion contiguous to the channel region and a second portion contiguous to the source or drain regions;

a gate insulating film formed over the semiconductor region;

a first conductive layer formed over the channel region with the gate insulating film interposed therebetween; and

a second conductive layer formed on the first conductive layer wherein a width of the first conductive layer is narrower than that of the second conductive layer,

wherein the second conductive layer extends beyond side edges of the first conductive layer and extending portions of

the second conductive layer overlap the first portions of said pair of regions while the second portions are not overlapped by said second conductive layer, and

wherein a distance between the first portion and the source or drain region is equal to or less than a thickness of the first conductive layer.

49. (NEW) A semiconductor device according to claim 1,

wherein a anodic oxide layer is formed on at least side surface of the first conductive layer and side surface of the second conductive layer.

50. (NEW) A semiconductor device according to claim 44,

wherein a anodic oxide layer is formed on at least side surface of the first conductive layer and side surface of the second conductive layer.

51. (NEW) A semiconductor device according to claim 45,

wherein an anodic oxide layer is formed on at least side surfaces of the first conductive layer and side surfaces of the second conductive layer.

52. (NEW) A semiconductor device according to claim 46,

wherein an anodic oxide layer is formed on at least side surfaces of the first conductive layer and side surfaces of the second conductive layer.

53. (NEW) A semiconductor device according to claim 47, wherein an anodic oxide layer is formed on at least side surfaces of the first conductive layer and side surfaces of the second conductive layer.

54. (NEW) A semiconductor device according to claim 48, wherein an anodic oxide layer is formed on at least side surfaces of the first conductive layer and side surfaces of the second conductive layer.

55. (NEW) A semiconductor device according to claim 1, wherein each of the first and second conductive layers comprises a material selected from the group consisting of molybdenum, tantalum, aluminum, chromium, nickel, zirconium, titanium, palladium, silver, copper, and cobalt.

56. (NEW) A semiconductor device according to claim 44,

wherein each of the first and second conductive layers comprises a material selected from the group consisting of molybdenum, tantalum, aluminum, chromium, nickel, zirconium, titanium, palladium, silver, copper, and cobalt.

57. (NEW) A semiconductor device according to claim 45, wherein each of the first and second conductive layers comprises a material selected from the group consisting of molybdenum, tantalum, aluminum, chromium, nickel, zirconium, titanium, palladium, silver, copper, and cobalt.

58. (NEW) A semiconductor device according to claim 46, wherein each of the first and second conductive layers comprises a material selected from the group consisting of molybdenum, tantalum, aluminum, chromium, nickel, zirconium, titanium, palladium, silver, copper, and cobalt.

59. (NEW) A semiconductor device according to claim 47, wherein each of the first and second conductive layers comprises a material selected from the group consisting of molybdenum, tantalum, aluminum, chromium, nickel, zirconium, titanium, palladium, silver, copper, and cobalt.

60. (NEW) A semiconductor device according to claim 48, wherein each of the first and second conductive layers comprises a material selected from the group consisting of molybdenum, tantalum, aluminum, chromium, nickel, zirconium, titanium, palladium, silver, copper, and cobalt.

61. (NEW) A semiconductor device according to claim 1, wherein a distance between the first portion and the source or drain region is 500. to 1000..

62. (NEW) A semiconductor device according to claim 44, wherein a distance between the first portion and the source or drain region is 500Å to 1000Å.

63. (NEW) A semiconductor device according to claim 45, wherein a distance between the first portion and the source or drain region is 500Å to 1000Å.

64. (NEW) A semiconductor device according to claim 46, wherein a distance between the first portion and the source or drain region is 500Å to 1000Å.

65. (NEW) A semiconductor device according to claim 47,

wherein a distance between the first portion and the source or drain region is 500Å to 1000Å.

66. (NEW) A semiconductor device according to claim 48, wherein a distance between the first portion and the source or drain region is 500Å to 1000Å.

67. (NEW) A semiconductor device according to claim 1, wherein said gate insulating film comprises silicon oxide.

68. (NEW) A semiconductor device according to claim 44, wherein said gate insulating film comprises silicon oxide.

69. (NEW) A semiconductor device according to claim 45, wherein said gate insulating film comprises silicon oxide.

70. (NEW) A semiconductor device according to claim 46, wherein said gate insulating film comprises silicon oxide.

71. (NEW) A semiconductor device according to claim 47, wherein said gate insulating film comprises silicon oxide.

72. (NEW) A semiconductor device according to claim 48, wherein said gate insulating film comprises silicon oxide.

73. (NEW) A semiconductor device according to claim 1, wherein said first conductive layer comprises tantalum and said second conductive layer comprises aluminum.

74. (NEW) A semiconductor device according to claim 44, wherein said first conductive layer comprises tantalum and said second conductive layer comprises aluminum.

75. (NEW) A semiconductor device according to claim 45, wherein said first conductive layer comprises tantalum and said second conductive layer comprises aluminum.

76. (NEW) A semiconductor device according to claim 46, wherein said first conductive layer comprises tantalum and said second conductive layer comprises aluminum.

77. (NEW) A semiconductor device according to claim 47, wherein said first conductive layer comprises tantalum and said second conductive layer comprises aluminum.

78. (NEW) A semiconductor device according to claim 48, wherein said first conductive layer comprises tantalum and said second conductive layer comprises aluminum.

79. (NEW) A semiconductor device according to claim 1, wherein the semiconductor region comprises crystalline silicon.

80. (NEW) A semiconductor device according to claim 44, wherein the semiconductor film comprises crystalline silicon.

81. (NEW) A semiconductor device according to claim 45, wherein the semiconductor region comprises crystalline silicon.

82. (NEW) A semiconductor device according to claim 46, wherein the semiconductor film comprises crystalline silicon.

83. (NEW) A semiconductor device according to claim 47, wherein the semiconductor region comprises crystalline silicon.

84. (NEW) A semiconductor device according to claim 48, wherein the semiconductor film comprises crystalline silicon.